Abstract of the Disclosure

A semiconductor device which is capable of avoiding an increase in pattern ratio and allowing wiring dummy patterns to improve global steps developed by CMP upon insertion of the dummy patterns which are different from an actual wiring pattern. The semiconductor device has a configuration wherein a gate wiring pattern is formed on a semiconductor substrate, a plurality of dummy patterns are provided therearound, and a BPSG oxide film which is flattened by CMP is formed on the gate wiring pattern and the dummy patterns as an interlayer insulating film. In the semiconductor device, the dummy patterns are formed so as to include pattern non-forming regions such as slits.